# Analog Predistortion High Power Amplifier Using Novel Low Memory Matching Topology

Jangheon Kim[1] · Young Yun Woo[2] · Jeonghyeon Cha[3] · Sungchul Hong[2] · Ildu Kim[1] · Junghwan Moon[1] · Jungjoon Kim[1] · Bumman Kim[1]

## Abstract

This paper represents an analog predistortion linearizer for the high power amplifier with low memory effect. The high power amplifier is implemented using a 90-W peak envelope power(PEP) LDMOSFET at 2.14-GHz and an envelope short matching topology is applied at the active ports to minimize the memory effect. The analog predistortion circuit comprises the fundamental path and the cuber and quintic generating circuits, whose amplitudes and phases can be controlled independently. The predistortion circuit is tested for two-tone and wide-band code division multiple access(WCDMA) 4FA signals. For the WCDMA signal, the adjacent channel leakage ratios(ACLRs) at 5 MHz offset are improved by 12.4 dB at average output powers of 36 dBm and 42 dBm.

*Key words* : Ajacent Channel Leakage Ratio(ACLR), Linearization, Memory Effect, Predistortion, Wide-Band Code Division Multiple Access(WCDMA).

## I. Introduction

Current wireless communication systems, such as code division multiple access(CDMA)-2000, wide-band code division multiple access(WCDMA), orthogonal frequency division multiplexing(OFDM) and so on, are progressed to increase the bandwidth and number of carriers for high data rates. The instantaneous transmit powers of the systems vary widely and rapidly, generating high peak-to-average power ratio(PAPR) signals. Power amplifiers for the systems require high linearity to amplify the signals without distortions. In order to satisfy the linearity specification, various linearization techniques are adopted. Among the techniques, an analog predistortion technique is preferred for the linear amplifiers due to the advantages of a simple structure, low cost, and reasonably good linearity improvement. However, because the power amplifiers have serious memory effects due to wide bandwidth characteristics of the systems, it is very difficult to apply the analog predistortion technique [1]~[4].

The memory effects are defined as changes of the amplitude and phase in distortion components due to the previous signals. To characterize them, two-tone signals with varying tone spacings are applied to an amplifier. The memory effects cause asymmetrical and tone spacing dependent intermodulation distortion(IMD) charac-

teristics[4]~[6]. An usual predistorter can not compensate the non-uniform charcateristics of the amplifiers because the predistorter has uniform IMD characteristics according to the tone spacing. Therefore, the memory effects of the high power amplifiers should be minimized in order to have a good harmonic cancellation behavior using the predistortion circuit.

Many previous works have tried to analyze the memory effects or reduce them, and they have found that the envelope impedance is the most important factor for reducing the memory effects[4]~[6]. However, the effects are still a big problem for the current high power amplifiers. The objective of this paper is to demonstrate a good performance of an analog predistorter for the power amplifiers with low memory effect. First, we have discussed the matching topology to reduce the memory effect. The matching topology consists of the tantalum capacitors at the gate and drain ports with the conventional matching circuit. The tantalum capacitors play an important role in shorting the envelope voltage components while providing matchable impedances at the fundamental frequency. Second, we have developed an analog cuber and quintic predistortion circuit that can control the IM3 and IM5 separately and applied it for the linearization of the low memory power amplifier. Third, we have also developed the analog predistortion power amplifier for a repeater system using the predis-

torter and the power amplifier with low memory effect. The amplifiers are tested for two-tone and WCDMA 4FA signals. The measurement results show that the power amplifiers with low memory effect are suitable for the linearization using the analog predistortion circuit.

## Ⅱ. The Matching Scheme for High Power Amplifier with Low Memory Effect

The envelope voltage components of $(f_2-f_1)$ and the second harmonic components of $2f_2$ and $2f_1$ generated by the nonlinearity of the amplifier cause the memory effects. The second harmonic components are removed by properly designing the bias circuit. However, it is difficult to remove the envelope components. Fig. 1 shows the circuit topologies for the conventional amplifier and the low memory amplifier. From Fig. 1(a), in order to explore the envelope components, the impedances of the gate and drain nodes can be represented by

$$Z_{Gate}(f_2-f_1)=Z_{G,device}\,/\!/\,Z_{G,match}\,/\!/\,Z_{G,bias} \qquad (1)$$

and

$$Z_{Drain}(f_2-f_1)=Z_{D,device}\,/\!/\,Z_{D,match}\,/\!/\,Z_{D,bias}. \qquad (2)$$

At the envelope frequency, the matching impedances $Z_{match}$ is nearly an open circuit, and the envelope impedance of each node depends on the impedances of the $Z_{bias}$[5]. As the power capacity of the power amplifier increases, the output load impedance of the amplifier decreases. It is difficult to short the envelope voltage component using the bias circuit because the reduced device impedance is very small and the envelope impedance of the bias circuits with $\lambda/4$ can be larger than the device impedance.

Fig. 1(b) shows the new matching topology to reduce the memory effect. The envelope voltage signal components are shorted right at the gate and drain terminals using large tantalum capacitors. In order to explore the envelope impedance of this matching topology, the impedance of each node can be calculated by

$$Z_{Gate}(f_2-f_1)=Z_{G,device}\,/\!/\,Z_{G,bias}\,/\!/\,Z_{G,env} \qquad (3)$$

and

$$Z_{Drain}(f_2-f_1)=Z_{D,device}\,/\!/\,Z_{D,bias}\,/\!/\,Z_{D,env}. \qquad (4)$$

Because the impedance of the envelope trap, $Z_{env}$, is close to a short at the envelope frequency and open at the RF, the envelope voltage components do not exist and the envelope trap circuit do not affect the fundamental load matching circuit. Therefore, high power amplifiers can be designed properly while reducing the



(a) Conventional amplifier
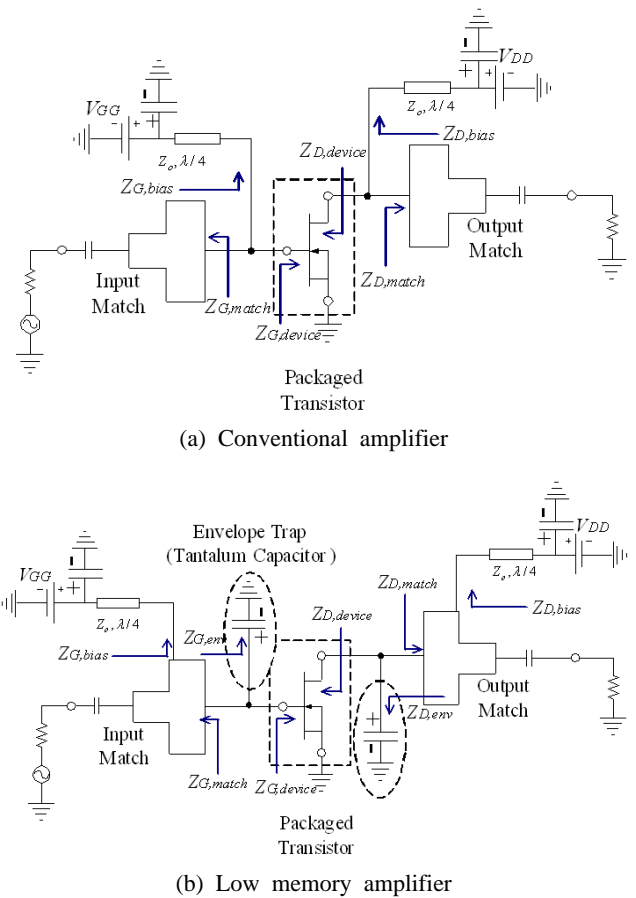


(b) Low memory amplifier

Fig. 1. Schematic diagram of high power amplifiers.

memory effect using the new topology.

We have implemented the power amplifiers on RF35 printed circuit boards, one is the conventional power amplifier and the other is the power amplifier with low memory effect, at 2.14-GHz using the Freescale MRF5-S21090. The device is able to deliver a 90 watt peak envelope power(PEP). The two power amplifiers have been optimized for the similar performance in linearity for WCDMA 4FA signal at the same bias point, $V_{DD}$ =27 V and $I_{DSQ}$=850 mA. The matching circuit of the amplifier with low memory effect comprises the tantalum capacitors (22 uF) located within each matching circuit as shown in Fig. 1(b).

## Ⅲ. Analog Predistortion Linearization Circuit

Fig. 2 shows a block diagram of the analog predistortion linearization circuit. An excited input signal is divided into the fundamental path, the cuber generating path, and the quintic generating path by two 3-dB hybrid couplers. At the cuber generating path(middle path), an excited input signal is applied to the cuber generating circuit, which creates the IM3 component using Shottky diodes. It can effectively cancel the fundamental
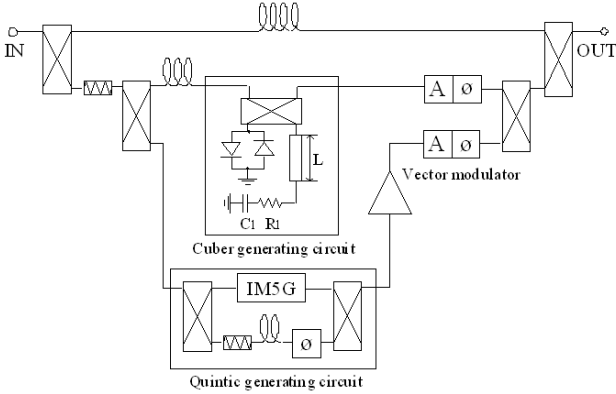
Fig. 2. Block diagram of the analog cuber and quintic pre-
distortion circuit.

signal by selecting a proper length of the transmission
line, resistor, and capacitor[2],[4].

At the quintic generating path(lower path), an excited
input signal is divided into the IM5 generating circuit
(IM5G) and the fundamental cancelling path. The circuit
configuration of the IM5G is similar to the cuber gene-
rating circuit as shown in Fig. 3(a). The biased Shottky
diodes of the IM5G induce the sweet spot for IM3
component, and the IM5 is larger than the IM3 compo-
nent for power range of 8 dB as shown in Fig. 3(b).
To generate only the IM5, the fundamental signal is can-
celled by the cancelling loop in the the quintic gene-
rating circuit. After generating the IM3 and IM5 com-
ponents, the IM5 component is amplified, and their am-
plitudes and phases are controlled by the vector modu-
lators consisting of a voltage variable attenuator and phase
shifter. These controlled IM3 and IM5 components are
combined with the delayed fundamental signal by two
3-dB couplers. Finally, the combined signals are supp-
lied to the power amplifier stage.

To validate the analog predistortion circuit, the analog
cuber and quintic generating circuits are implemented,
and Fig. 4 shows a photograph of the analog predis-
torter. The cuber generating circuit consists of Shottky
diodes (Hewlett-Packard HSMS2850), transmission line
with electrical length($L$) of 0.12 $\lambda$, $R_1$=5.1 $\Omega$, and $C_1$
=2.7 pF. The IM5 generating circuit also comprises
Shottky diodes, $R_2$=8.2 $\Omega$, $C_2$=3.9 pF, $C_3$=10 pF, $R_3$=
2 k$\Omega$, and the bias voltage $V_{dc}$=0.3 V as shown in Fig.
3(a).

## Ⅳ. Experimental Results

Fig. 5 illustrates the IMD3 characteristics of each am-
plifier for two-tone (up to 20 MHz tone spacing) signal.
As shown in Fig. 4, the IMD3 difference (IM3U-IM3L)
of the conventional amplifier increases according to the
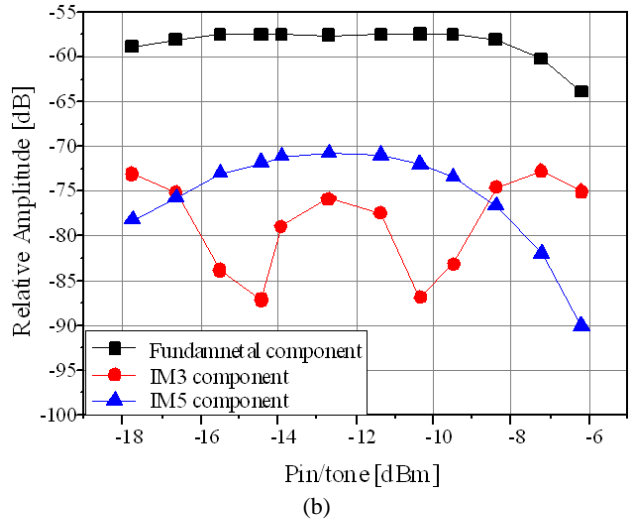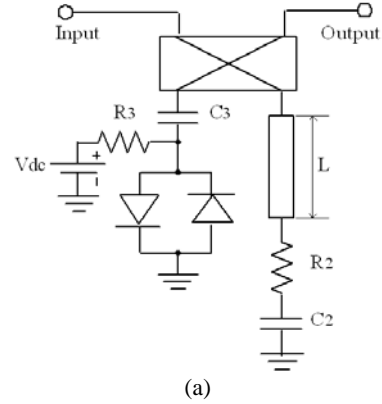


(a)



(b)

Fig. 3. (a) Block diagram of the IM5 generating circuit
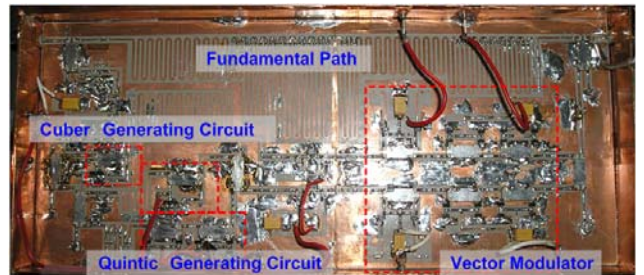(IM5G). (b) Measured fundamental, 3rd, and 5th
components generated by IM5G.



Fig. 4. Photograph of the analog cuber and quintic pre-
distortion circuit.

tone spacing, but the IMD3 characteristic of the ampli-
fier with low memory effect is not affected by the spa-
cing. Moreover, the IMD3s are not monotonous over
the whole output power range.

These experimental results show the proposed mat-
ching topology is effective for reducing the envelope
frequency components, and the amplifier is suitable for
applying the analog predistortion linearization circuit due
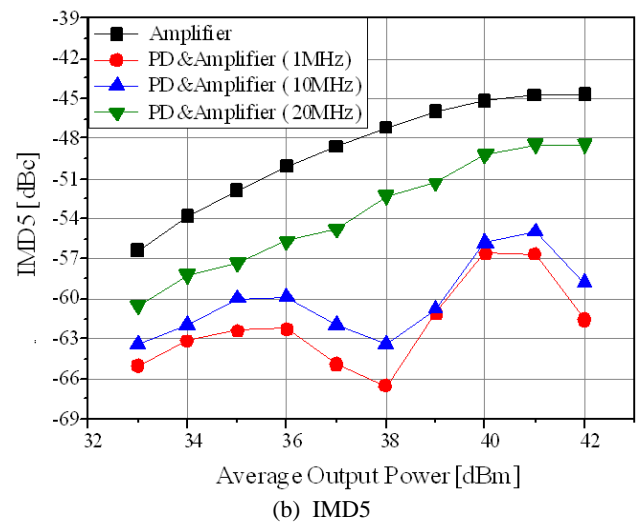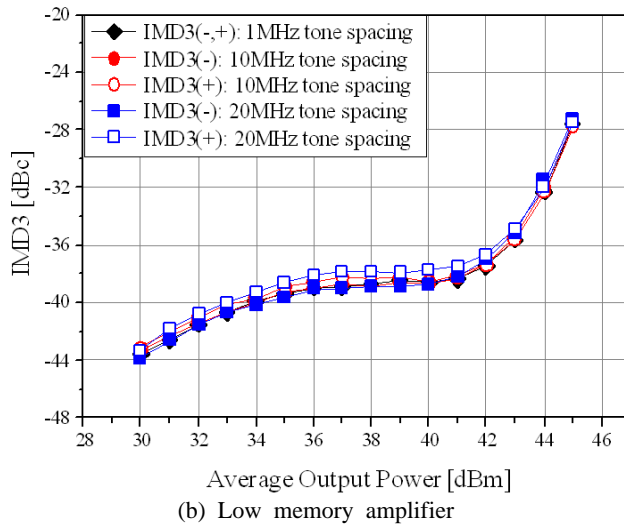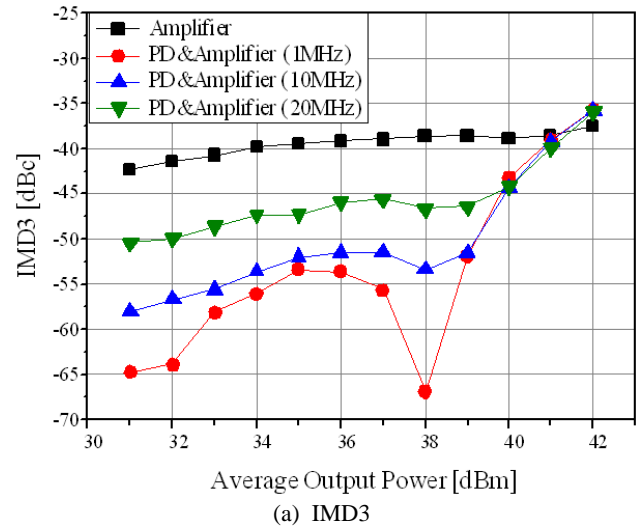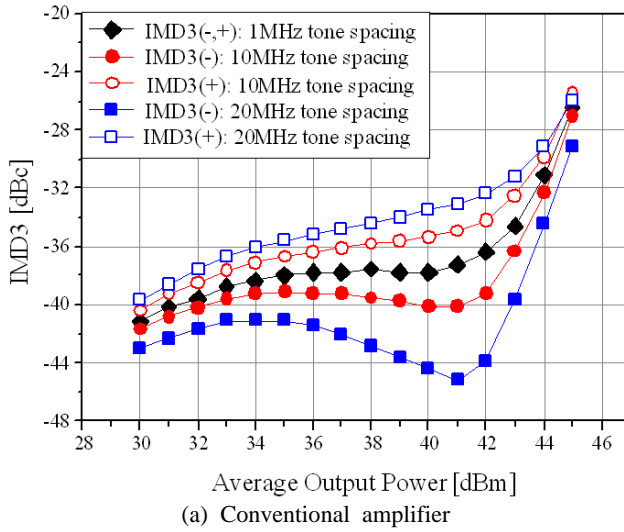
(a) Conventional amplifier



(b) Low memory amplifier

Fig. 5. Measured IMD3 performance of each amplifier for two-tone (up to 20 MHz tone spacing) signal.



(a) IMD3



(b) IMD5

Fig. 6. Measured IMD performance before and after the linearization of the amplifier with low memory effect for two-tone (up to 20 MHz tone spacing) signal.

to such low memory characteristic.

Fig. 6 shows the IMD characteristics, before and after the linearization, of the power amplifier with low memory effect for a two-tone (up to 20 MHz tone spacing) signal. We could linearize the distortions significantly, more than 13 dB up to 10 MHz tone spacing signal, but the improvement is reduced to 7~8 dB for 20 MHz tone spacing signal.

In order to explore the linearization performance of the analog predistortion circuit for WCDMA 4FA signal with a 20 MHz bandwidth, the proposed predistortion circuit is optimized at an average output power of 36 dBm. Due to the high PAPR of the WCDMA 4FA signal, the analog predistortion circuit should be optimized at 38 dBm for a two-tone signal. Fig. 7 shows the measured adjacent channel leakage ratio(ACLR) performance, before and after linearization, of the amplifier for WCD-

MA 4FA signal. The ACLRs at 5 MHz offset and at 10 MHz offset are improved by 12.4 dB and 11.5 dB, respectively, at the average output power of 36 dBm. This experimental result indicates that the linearization performance of WCDMA 4FA signal with a 20 MHz bandwidth depends on the linearization of the two-tone signal up to 10 MHz tone spacing.

Fig. 8 shows the power amplifier line-up for a repeater system using the analog cuber and quintic predistorter, configured to generate a 15-W (42 dBm) average output power for WCDMA 4FA signal. The main amplifier is comprised by two identical power amplifiers with low memory effect represented in Section II and is combined by 3-dB hybrid coupler at the input and output ports. Fig. 9 shows the measured ACLR per-
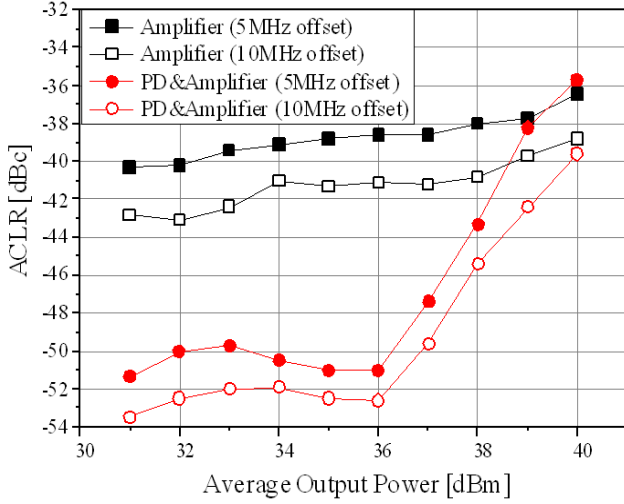
Fig. 7. Measured ACLR performance before and after the linearization of the amplifier with low memory effect for WCDMA 4FA signal.
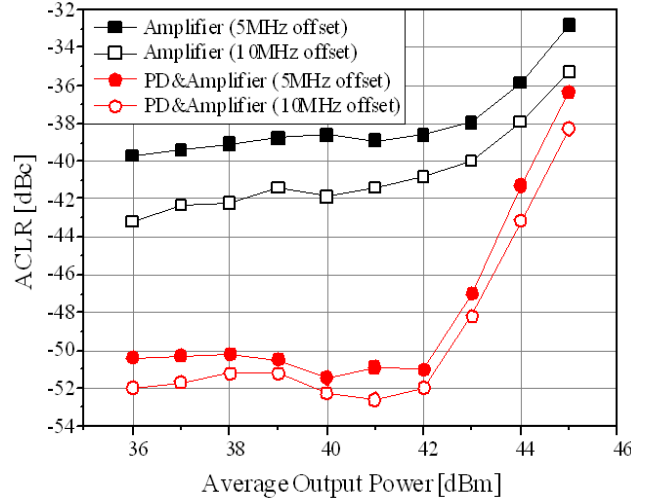


Fig. 9. Measured ACLR performance of the low memory and analog predistortion power amplifiers for WCD-MA 4FA signal.
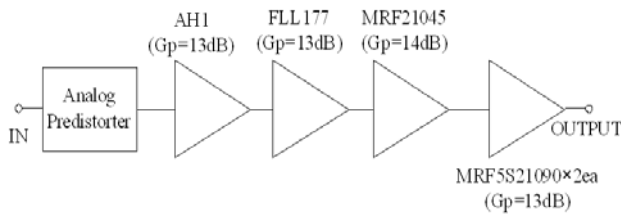


Fig. 8. Line-up of the analog predistortion power amplifier for a repeater system.



Fig. 10. Measured WCDMA 4FA spectra of the low memory and analog predistortion power amplifiers at an average output power of 42 dBm.

formance before and after linearization of the predistortion power amplifier for WCDMA 4FA signal. The ACLRs at 5 MHz offset and at 10 MHz offset are improved by 12.4 dB and 11.2 dB, respectively, at the average output power of 42 dBm. Contrary to the low memory amplifier, the conventional power amplifiers do not produce any significant ACLR cancellation, less than 2 dB linearization. The total efficiency of the analog cuber and quintic predistortion circuit and amplifiers is 9.5 % at the average output power of 42 dBm. Fig. 10 shows the measured spectra before and after linearization of the predistortion power amplifier at an average output power of 42 dBm.

## Ⅴ. Conclusions

We have developed a high power amplifier with low memory effect suitable for the analog predistortion linearization circuit. The high power amplifier is implemented using a 90-W PEP LDMOSFET at 2.14-GHz and the envelope short matching topology is applied at the gate and drain ports to minimize the memory effect.
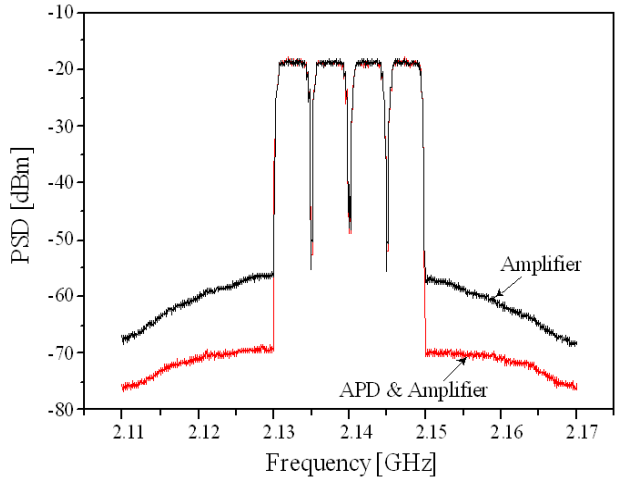
The analog predistortion circuit consists of the fundamental path and the cuber and quintic generating circuits, and can be controlled independently for the amplitudes and phases of the distortion components. To validate the linearization performances of the proposed amplifier experimentally, we applied the analog predistortion linearization circuit. For WCDMA 4FA signal, the ACLRs at 5 MHz offset are improved by 12.4 dB at average output powers of 36 dBm and 42 dBm, contrary to the under 2 dB improvement for a conventional power amplifier. These experimental results show that the amplifier with low memory effect is suitable for the linearization using the analog predistortion circuit.

## References

[1] P. B. Kenington, *High-Linearity RF Amplifier Design*, Norwood, MA: Artech House, 2000.

[2] T. Nojima, T. Konno, "Cuber predistortion linearizer for relay equipment in 800 MHz band land mobile telephone system", *IEEE Trans. Veh. Technol.*, vol. VT-34, pp. 169-177, Nov. 1985.

[3] J. Yi, Y. Yang, M. Park, W. Kang, and B. Kim, "Analog predistortion linearizer for high power RF amplifier", *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 12, pp. 2709-2713, Dec. 2000.

[4] J. Cha, J. Yi, J. Kim, and B. Kim, "Optimum design of a predistortion RF power amplifier for multicarrier WCDMA applications", *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 2, pp. 655-663, Feb. 2004.

[5] J. Vuolevi, T. Rahkonen, *Distortion in RF Power Amplifiers*, Norwood, MA: Artech House, 2003.

[6] A. Rabany, L. Nguyen, and D. Rice, "Memory effect reduction for LDMOS bias circuits", *Microw. J.*, vol. 46, no. 2, Feb. 2003.

## Jangheon Kim
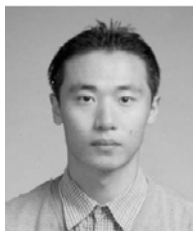
received the B.S. degree in electronics and information engineering from Chonbuk National University, Chonju, Korea, in 2003. He is currently working toward Ph.D. degree in Pohang University of Science and Technology(POSTECH), Pohang, Korea. His current research interests include highly linear and efficient RF PA design, memory effect compensation techniques, and digital predistortion(DPD) techniques.

## Jeonghyun Cha

was born in Gimje, Korea, in 1975. He received the B.S. degree in electronics and information engineering from Chonbuk National University, Chonju, Korea, in 2001, and the Ph.D. degree in electrical engineering from the Pohang University of Science and Technology(POSTECH), Pohang, Gyungbuk, Korea, in 2007. In 2005, he joined the XRONet Corporation, Seongnam, Gyeonggi, Korea. His current research interests include Phase-Locked Loop(PLL) frequency synthesizers, RF transceivers, and PAs for wireless communications.

## Young Yun Woo

received the B.S. degree in electrical and computer engineering from Han-yang University, Seoul, Korea, in 2000 and Ph.D. degree in electronic and electrical engineering from the Pohang University of Science and Technology(POSTECH), Pohang, Korea, in 2007. In 2007, he joined the Samsung Electronics Company Ltd., Suwon, Gyeunggi, Korea. His current research interests include RF power amplifier design, linear power amplifier(LPA) system design, and digital predistortion(DPD) techniques for linearizing high power amplifiers.

## Sungchul Hong

received his B.S. degree in electrical and electronic engineering from the Yonsei University, Seoul, Korea, in 2003 and the Master degree in electronic and electrical engineering from Pohang University of Science and Technology(POSTECH), Pohang, Korea in 2007. In 2007, he joined the Samsung Electronics Company Ltd., Suwon, Gyeunggi, Korea. His research interests include design of power amplifiers, digital predistortion(DPD) techniques, and highly efficient transmitter systems.

**Ildu Kim**

was born in Kwangju, Korea, in 1981. He received the B.S. degree in electronics and information engineering from Chonnam National University, Kwangju, Korea, in 2004, and is currently working toward the Ph.D. degree at the Pohang University of Science and Technology(POSTECH), Pohang, Gyeongbuk, Korea. His current research interests include highly linear and efficient RF PAs and transmitter design for basestation.

**Jungjoon Kim**
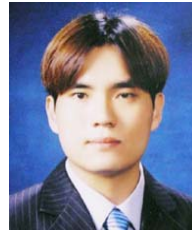
was born in Seoul, Korea, in 1981. He received the B.S. degree in electrical engineering from Hanyang University, Ansan, Korea, in 2007, and is currently working toward the M.S. degree at the Pohang University of Science and Technology(POSTECH), Pohang, Gyungbuk, Korea. His current research interests include RF power amplifier design and linearity and efficiency improvement techniques.

**Junghwan Moon**

received the B.S. degree in electrical and computer engineering from University of Seoul, Seoul, Korea, in 2006, and is currently working toward the Ph.D. degree at the Pohang University of Science and Technology(POSTECH), Pohang, Gyungbuk, Korea. His current research interests include highly linear and efficient RF PA design, memory effect compensation techniques, and digital predistortion(DPD) techniques.

**Bumman Kim**

received the Ph.D. degree in electrical engineering from Carnegie. Mellon University, Pittsburgh, PA, in 1979. From 1978 to 1981, he was engaged in fiber-optic network component research with GTE Laboratories Inc. In 1981, he joined the Central Research Laboratories, Texas Instruments Incorporated, where he was involved in development of GaAs power field-effect transistors (FETs) and monolithic microwave integrated circuits(MMICs). He has developed a large-signal model of a power FET, dual-gate FETs for gain control, high-power distributed amplifiers, and various millimeter-wave MMICs. In 1989, he joined the Pohang University of Science and Technology(POSTECH), Pohang, Gyungbuk, Korea, where he is a Namko Professor with the Department of Electrical Engineering, and Director of the Microwave Application Research Center, where he is involved in device and circuit technology for RF integrated circuits(RFICs). He was a Visiting Professor of electrical engineering with the California Institute of Technology, Pasadena, in 2001. He has authored over 200 technical papers. Dr. Kim is a member of the Korean Academy of Science and Technology and the Academy of Engineering of Korea. He was an associate editor for the IEEE Transactions on Microwave Theory and Techniques and a Distinguished Lecturer of the IEEE Microwave Theory and Techniques Society(IEEE MTT-S).