Improving the Linearity of CMOS LNA Using the Post IM3 Compensator

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Abstract

In this paper, a new linearization method has been proposed for a CMOS low noise amplifier(LNA) using the Post IM3 Compensator. The fundamental operating theory of the proposed method is to cancel the IM3 components of the LNA output signal by generating another IM3 components, which are out-phase with respect to that of the LNA, from the Post IM3 Compensator. A single stage common-source LNA has been designed to verify the linearity improvement of the proposed method through 0.13 μm RF CMOS process for WiBro system. The designed LNA achieves +7.8 dBm of input-referred 3rd-order intercept point (IIP3) with 13.2 dB of Power Gain, 1.3 dB of noise figure and 5.7 mA @1.5 V power consumption. IIP3 is compared with a conventional single stage common-source LNA, and it shows IIP3 is increased by +12.5 dB without degrading other features such as gain and noise figure.

Key words : Low Noise Amplifier, Post-IM3 Compensator, Linearity, IIP3.

Ⅰ. Introduction

The low noise amplifier(LNA) is the most important component to compensate the noise figure in a RF front-end module. The key design parameters of LNA are the high gain, the low noise figure(NF) and the high linearity. The linearity becomes more and more important in a modern digital wireless system because a complex digital modulation signal usually has a high peak-to-average power ratio. Therefore, a highly linear LNA is demanded in a wireless receiver to reduce its intermodulation distortion. The linearity in LNA is described by its input referred 3rd-order intercepter point (IIP3).

There have been some techniques to improve the linearity of LNA. One good example[1] is based on the modified derivative superposition method which cancels the 3rd-order intermodulation distortion of the main FET's by paralleling the auxiliary FET biased near the weak inversion region. This method is very attractive because it can increase linearity significantly with wide DC operating point range. Since the auxiliary FET biased in sub-threshold region generates more noise than the saturation-region biased one, however, it causes appreciable increase of noise figure. In another important result[2], Active post distortion(APD) method has been proposed using the drain of main FET. But that method consumes dc power excessively to improve the linearity.

In this paper, a new linearity improvement method, the post IM3 compensator, is proposed. To demonstrate its performance, a CMOS LNA has been designed for WiBro application which frequency range is from 2.3 GHz to 2.4 GHz. This approach does not need an auxiliar sub-threshold biased FET like [1]. Moreover, since the compensator is added to the output of LNA, this technique can improve the linearity without a significant gain and noise figure degradation.

Ⅱ. Post IM3 Compensator

2-1 Theory of IM3 Compensator

Fig. 1 shows the concept of the post IM3 compensator and the schematic of the post IM3 compensator is shown in Fig. 2. As shown in Fig. 1, the post IM3 compensator is connected to the output of LNA. The IM3 compensator generates 3rd-order nonlinear terms,

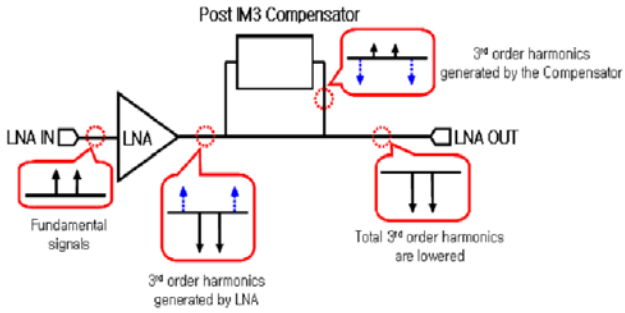

Fig. 1. Concept of the post IM3 compensator.

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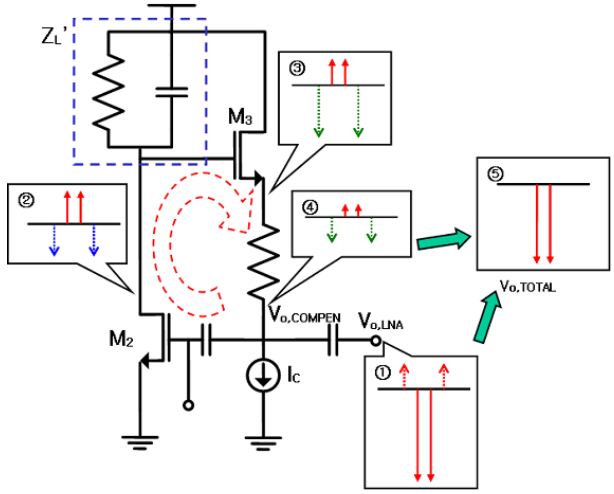

Fig. 2. The signal flow through the post IM3 compensator.

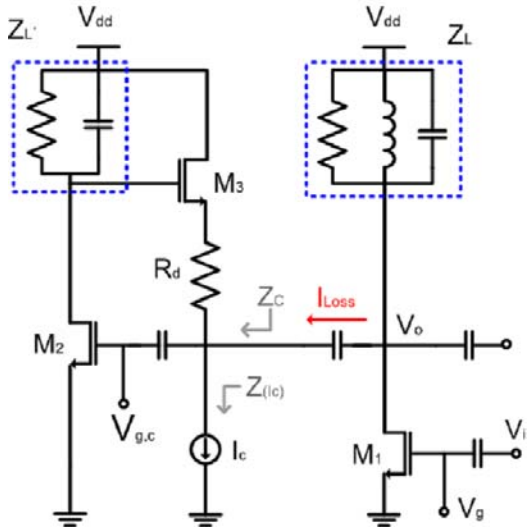

Fig. 3. Total architecture of single stage common-source LNA using the post IM3 compensator.

which are out-phase with respective to 3rd-order nonlinear terms of LNA output signal to reduce the combined 3rd-order nonlinear terms by cancellation of each other.

When the common source FET is operating in saturation mode, the small-signal output voltage of LNA can be expanded into the following power series in terms of the small-signal input voltage V_i:

$$V_{o,LNA}(V_i) = -(g_{m1}V_i + g_{m2}V_i^2 + g_{m3}V_i^3)Z_L \quad (1)$$

where

g_{m1} : the small-signal transconductance of LNA (>0)
g_{m2} : the first order derivative of g_{m1} (>0)
g_{m3} : the second order derivative of g_{m1} (<0)
Z_L : load impedance of LNA

In case of a weakly non-linear circuit such as LNA, the nonlinear terms higher than 3rd-order can be safely ignored. As shown in the equation (1), the fundamental components of LNA output are also out of phase with respective to its input fundamental signals. But the 3rd-order intermodulation terms of LNA output are in-phase with V_i, that is, both of them are out-phase with each other.

The operation of the post IM3 compensator can be demonstrated through the Fig. 2. $V_{o,LNA}$ and $V_{o,COMPEN}$ are the input and output signal of the IM3 compensator. The common source transistor, M2, generates 3rd-order distortion terms from the LNA output, $V_{o,LNA}$. The generated distortion terms are out of phase with the LNA output signal ①, and the signal ② is provided to the source follower transistor, M3. The source follower output ③ is attenuated by R_d which should be tuned to cancel 3rd-order distortion terms of the LNA output $V_{o,LNA}$. The circuit loop of the common source and source follower generates the required 3rd-order distortion terms, and the ratio of R_d to Z_L determines the amount of the combining distortion components as shown at ④ in Fig. 2. The output voltage of the post IM3 compensator can be modeled by the following power series:

$$V_{o,COMPEN} = -\alpha(g'_{m1}V_{o,LNA} + g'_{m2}V_{o,LNA}^2 + g'_{m3}V_{o,LNA}^3)Z'_L \quad (2)$$

where

g'_{m1} : the small-signal transconductance of the post IM3 compensator (>0)
g'_{m2} : the first order derivative of g'_{m1} (>0)
g'_{m3} : the second order derivative of g'_{m1} (<0)
α : the gain coefficient according to ratio of R_d to Z_L in the post IM3 compensator ($0<\alpha\leq 1$)
Z'_L : load impedance of the post IM3 compensator

Substituting the equation (1) into the equation (2), the equation (2) can be expressed in terms of V_i. The first-order approximation of $V_{o,LNA}$ is enough to show the cancellation mechanism in the 3rd-order intermodulation terms. Equation (3) shows the output terms of the post IM3 compensator circuit with first order approximation.

$$V_{o,COMPEN} \approx \alpha(-g'_{m1}g_{m1}Z_L V_i + g'_{m2}g_{m1}^2 Z_L^2 V_i^2 - g'_{m3}g_{m1}^3 Z_L^3 V_i^3)Z'_L \quad (3)$$

Finally, the generated 3rd-order intermodulation terms

are recombined with 3rd-order intermodulation of LNA at the output port of LNA(⑤ in Fig. 2).

$$\begin{aligned} V_{o,TOTAL} &= V_{o,LNA} + V_{o,COMPEN} \\ &= (g_{m1}Z_L - \alpha g'_{m1} g_{m1} Z_L Z'_L) V_i \\ &\quad + (g_{m2}Z_L + g'_{m2} g_{m1}^2 Z_L^2 Z'_L) V_i^2 \\ &\quad + (g_{m3}Z_L - \alpha g'_{m3} g_{m1}^3 Z_L^3 Z'_L) V_i^3 \end{aligned} \quad (4)$$

By adjusting α, Z'_L and g'_3 values of the post IM3 compensator, the 3rd-order intermodulation terms of total output signal can be decreased as:

$$IM3_{o,TOTAL} = (g_3 Z_L - \alpha g'_3 g_1^3 Z_L^3 Z'_L) V_i^3 \approx 0 \quad (5)$$

2-2 Other Performances Issues in Method

Intuitively, the degradation of noise figure is minor because the post IM3 compensator is used at the output port of LNA. Moreover, it is biased in strong inversion region so that it does not generate other non-linear terms.

On the other hand, there are some factors which affect the LNA gain. Those are described as:

- the fundamental components generated by the post IM3 compensator are out-phase with $V_{o,LNA}$ (④ in Fig. 2): their effect can become insignificant, however, by minimizing the size of M_2. As the size of M_2 is small, it generates not only less fundamental signal but also more 3rd-order intermodulation signal.
- an additional output signal power path (I_{Loss}): since some of the fundamental signal currents of LNA output flow into the input of the post IM3 compensator, the gain of LNA can be lowered.
- the low input impedance(Z_{Compen}): the source of M_3 is connected to the output of LNA through R_d and then the input impedance of the post IM3 compensator is low as:

$$\begin{aligned} Z_{Compen} &= (1/g_{m1,M3} + R_d) \parallel Z(I_c) \\ &\approx 1/g_{m1,M3} + R_d \end{aligned} \quad (6)$$

This low impedance causes a decrease of the output impedance of LNA so that the gain of LNA can be lowered.

Ⅲ. Design Results

A LNA has been designed based on the proposed architecture shown in Fig. 3 with additional switches to turn on/off the post IM3 compensator circuit. The switch controls the gate bias ($V_{g,c}$) and current source(I_c) of the post IM3 compensator. By turning off the post IM3 compensator, the designed LNA operates as a conventional single stage common-source LNA. In the simulation, it is found that the post IM3 compensator circuit disabled by turning off the switch has no effect on the performance of the conventional LNA.

The LNA is designed with 0.13 μm RF CMOS process. The simulated results show that the LNA using the post IM3 compensator has 13.2 dB of power gain, 1.3 dB of noise figure and +7.8 dBm of IIP3 (+21 dBm of OIP3) while consuming 5.7 mA current from 1.5 V power supply. The IM3 reduction is about −26 dB, which increases IIP3 performance by +12.5 dB, with only additional 0.9 mA current consumption.

The simulated results are shown in Fig. 4 to 7 and the performances are compared in Table 1. Fig. 4 and Fig. 5 show the gain and noise figure of the LNA. As can be seen, the gain loss is 1 dB and the noise figure loss is 0.1 dB. They show good agreement with the explanation in the section Ⅱ. The IIP3 performances are shown in Fig. 6 and Fig. 7. The simulated results show that the

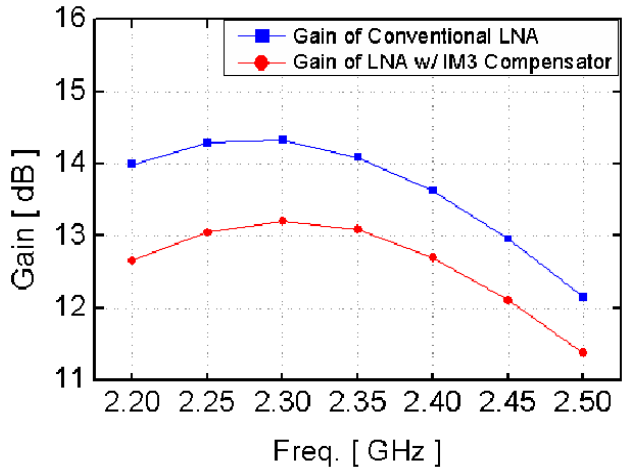

Fig. 4. Simulated gain curve.

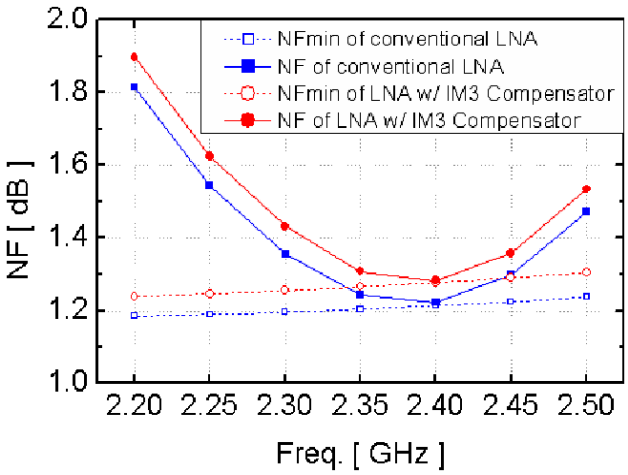

Fig. 5. Simulated noise figure curve.

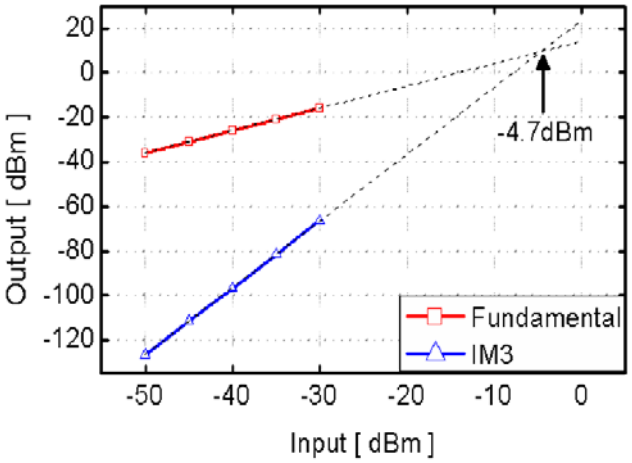

Fig. 6. Simulated IIP3 curve of conventional LNA @ 2.35 GHz.

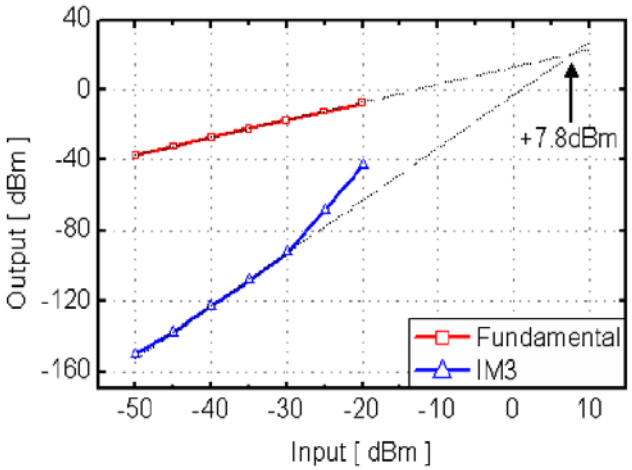

Fig. 7. Simulated IIP3 curve of LNA with the post IM3 compensator @ 2.35 GHz.

IIP3 improves +12.5 dB up to −30 dBm of input power. Table 1 summarizes and compares the performances of

Table 1. Summary of simulated results at 2.35 GHz.

	LNA using the Post IM3 Compensator	Conventional LNA
Gain (dB)	13.2	14.3
Idc(mA) @1.5 V	5.7	4.8
P1dB (dBm)	−9.4	−12.9
IIP3 (dBm)	7.8	−4.7
NF (dB)	1.3	1.2

LNAs at 2.35 Ghz. It shows that not only IIP3 but also P1dB is increased by 3.5 dB.

Ⅳ. Conclusion

In this paper, we proposed a new method to improve the linearity performance in a CMOS LNA using the post IM3 compensator method with the explanation, and a linearized single stage common-source LNA has been designed for WiBro system using the proposed technique. The design simulation results are compared with the conventional design results which show that the IIP3 performance improvement is by 12.5 dB without sacrificing other features such as noise figure and gain.

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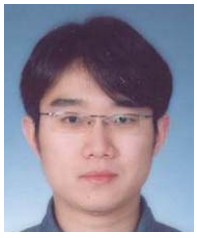

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