Gate-Bias Control Technique for Envelope Tracking Doherty Power Amplifier

Envelope Tracking 도허티 전력 증폭기의 Gate-Bias Control Technique

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Abstract

The gate-biases of the Doherty power amplifier are controlled to improve the linearity performance. The linearity improvement mechanism of the Doherty amplifier is the harmonic cancellation of the carrier and peaking amplifier at the output power combining point. However, it is difficult to cancel the harmonic power for the broader power range because the condition for cancelling is varied by power. For the linearity improvement, we have explored the linearity characteristic of the Doherty amplifier according to the input power and gate biases of the carrier and peaking amplifier. To extend the region of harmonic power cancellation, we have injected the proper gate bias to the carrier and peaking amplifier according to the input power levels. To validate the linearity improvement, the Doherty amplifier is designed using Eudyna 10-W PEP GaN HEMT EGN010MKs at 2.345 GHz and optimized to achieve a high linearity and efficiency at an average output power of 33 dBm, backed off about 10 dB from the P_{1dB}. In the experiments, the envelope tracking Doherty amplifier delivers a significantly improved adjacent channel leakage ratio performance of −37.4 dBc, which is an enhancement of about 2.8 dB, maintaining the high PAE of about 26 % for the WCDMA 1-FA signal at an average output power of 33 dBm. For the 802.16-2004 signal, the amplifier is also improved by about 2 dB, −35 dB.

요 약

본 논문에서는 선형성 증가를 위해 도허티 증폭기의 게이트 바이어스를 조정하는 방식을 제시하였다. 도허티 증폭기의 선형성 향상은 출력 결합 지점에서의 고조파 상쇄를 통해 이루어진다. 하지만 고조파의 상쇄는 그 크기와 위상이 출력 지점에서 같은 크기와 서로 다른 위상을 가지고 있어야 이루어질 수 있는데, 넓은 출력 전력 범위에서 위와 같은 조건을 만족시키는 것은 쉽지 않다. 선형성 증가를 위해 도허티 증폭기의 캐리어 증폭기와 피킹 증폭기의 선형성 특성을 입력 전력과 각 증폭기의 게이트 바이어스를 조정함으로써 살펴보았다. 살펴본 특성을 기본으로 하여 고조파 상쇄 전력 범위를 증가시키기 위해, 각 전력 레벨에 맞는 게이트 바이어스를 증폭기에 인가하였다. 게이트 바이어스 제어를 통한 선형성 향상을 알아보기 위해, 2.345 GHz에서 Eudyna사의 10-W PEP GaN HEMT EGN010MK 소자를 이용하여 도허티 전력 증폭기를 설계하였고, P_{1dB}로부터 10 dB back-off 지점인 33 dBm에서 고효율과 고선형성을 위해 최적화 되었다. WCDMA 1-FA 신호에 대해 제안된 게이트 바이어스 컨트롤 된 도허티 증폭기는 2.8 dB의 선형성 개선을 확인할 수 있었으며, 26 %의 PAE를 확인할 수 있었다.

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또한, 802.16-2004 신호에 대해 RCE가 2 dB 증가됨을 확인할 수 있었다.

Key words : Doherty Amplifier, Envelope Tracking, Gate Bias Control, GaN HEMT Amplifier, Linearity Improvement Technique, WCDMA, WiMAX

Ⅰ. Introduction

Current and next generation communication systems are required to transmit amount of data for various contents. As a result, the signals of the systems have large peak-to-average power ratios(PAPRs) caused by complex modulation scheme to efficiently use the frequency resource. To amplify these signals linearly, the power amplifier(PA) should be operated at a large backed-off output power region, which cause the degradation of efficiency performance. To improve the efficiency of the PA, many techniques are proposed recently, such as envelope tracking, envelope elimination and restoration, and so on. Among them, the Doherty PA is a good choice for the modern communication systems because of high efficiency performance at the large backed-off power levels with simple circuit topology and many researches are verified this. Moreover, a harmonic cancellation mechanism between the carrier and peaking amplifier of the Doherty topology using the derivative superposition method improved the linearity performance[1]~[3]. However, it is difficult to satisfy the harmonic cancellation conditions over the broader power levels since the conditions are changed by various elements, such as input power level and gate bias of each amplifier[4].

To extend the harmonic cancellation power ranges and improve the linearity performance of the Doherty PA, we have proposed the Doherty amplifier employing the gate-bias control technique according to the magnitude of the envelope signal, which is described in section II. To verify the linearity improvement through the extension of the harmonic cancellation power regions, we have simulated on the advanced design system (ADS) using Freescales 4-W PEP LDMOSFET MRF-281SR1s at the 2.14 GHz and experimented using Eudyna 10-W PEP GaN HEMT EGN010MKs at the 2.345 GHz. Based on a two-tone test, we have selected the proper gate biases of the carrier and peaking amplifiers according to the power level, and then we have injected the proper gate biases to the carrier and peaking amplifiers. For the WCDMA-1FA and IEEE 802.16-2004 signal test, the improved linearity performances of the envelope tracking Doherty amplifier employing gate bias control technique are demonstrated.

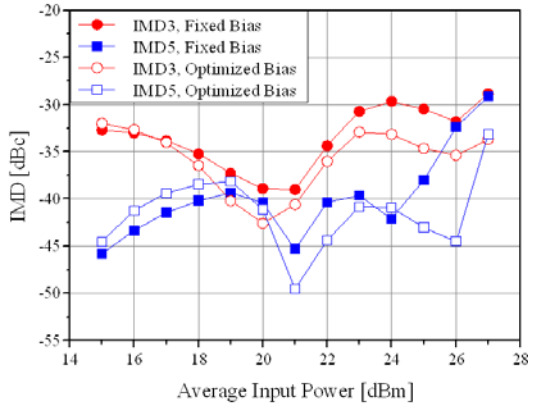
Ⅱ. Gate Bias Control by Employing Envelope Tracking Technique

It is well known that the linearity improvement mechanism of the Doherty PA is cancellation of the third-order inter-modulation(IM3) between the carrier and peaking amplifiers. When the IM3 characteristics of the amplifiers are perfectly satisfied with the equations (1) and (2), the IM3 power is cancelled out maximally at the output combining point of the Doherty topology,

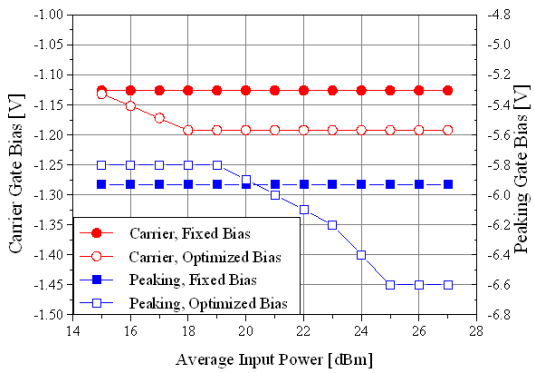
$$|IM3_C| = |IM3_P| \tag{1}$$

$$\angle IM3_C = \angle IM3_P \pm \pi . \tag{2}$$

However, the IM3 magnitude and phase of each amplifier are functions of the gate bias, power level, and so on, so it is very difficult to satisfy the conditions of equations (1) and (2) for the wide power ranges. To extend the IM3 cancellation power regions of the Doherty amplifier, we have selected the proper gate biases for each input power level. Figs. 1(a) and (b) show the measured inter-modulation distortion(IMD) characteristics with and without gate bias adaptation according to the power levels and selected gate biases of each amplifier for the two-tone signal with 1 MHz tone spacing. The gate biases are selected for optimizing the IMD3 characteristic at each power level and controllable sha-



(a)



(b)

Fig. 1. (a) Measured IMD characteristics with and without gate bias control. (b) Gate biases of the carrier and peaking amplifiers for optimizing the IMD3 characteristic.

pes. By adjusting the gate biases, we could obtain more linear characteristic over the broader power levels.

Ⅲ. Simulation and Experimental Results

3-1 Simulation Results

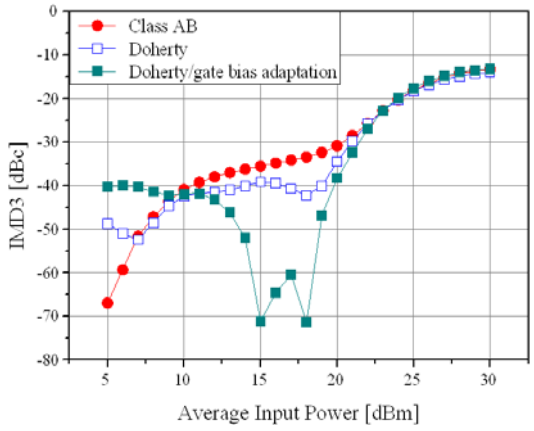
For verifying the linearity improvement using the gate-bias envelope tracking, we have simulated on ADS 2004A. The simulated Doherty amplifier is designed using two cells of Freescales 4-W peak envelope power LDMOSFET MRF281SR1s. The amplifier handles about 40 dBm of P_{1dB} at 2.14 GHz and was optimized to achieve high linearity and efficiency at an average output power of 30 dBm.

Figs. 2(a) and (b) show the simulated IMD characteristics of the class-AB and Doherty PA with and without gate bias adaptation, and gate biases of the carrier and peaking amplifiers. From the Fig. 2(a), we can recognize more linear characteristic of the gate-bias adapted Doherty amplifier than others. Fig. 2(c) shows the simulated adjacent channel leakage ratio(ACLR) performance of the class-AB and Doherty amplifiers with and without gate bias control for the CDMA signal with PAPR of about 10 dB. As expected, ACLR performance of the proposed Doherty amplifier is enhanced over the border output power ranges, thanks to the extension of the IM3 cancellation power regions.

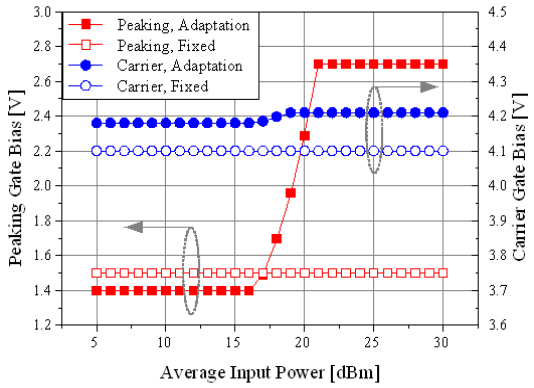
3-2 Experimental Results

To validate the linearity improvement employing the gate-bias envelope tracking, we have designed the Doherty amplifier using Eudyna 10-W peak envelope power GaN HEMT EGN010MKs. The amplifier can handle a 43 dBm of P_{1dB} at 2.345 GHz. In the experiments, the quiescent biases and individual matching circuitry of the carrier and peaking amplifiers are selected to maximally cancel the ACLR performance at an average output power of 33 dBm, backed-off about 10 dB from the P_{1dB}.

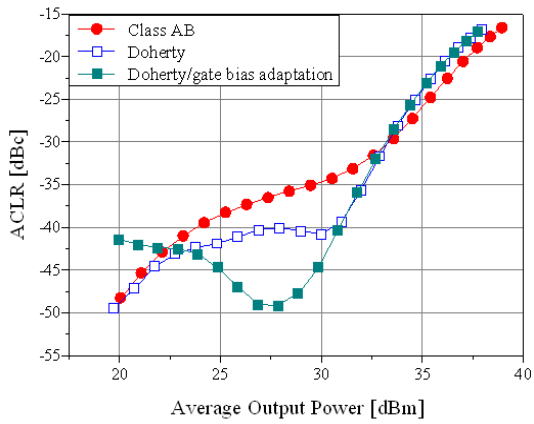
Fig. 3 shows the experimental setup for gate-bias envelope tracking experiment, which consists of ADS as an I and Q data source for WCDMA 1-FA signal and IEEE 802.16-2004 fixed WiMAX signal, MATLAB as a digital signal processor(DSP) for shaping the gate biases of the carrier and peaking amplifiers, ESG E4438C as a modulator for WCDMA 1-FA and IEEE 802.16-2004 signal sources, and PSG E8267D as a digital to analog converter(DAC) for the shaped gate bias sources. The output signal of DAC is amplified or shifted by differential OP-AMP voltage amplifiers. Then, the gate bias signals are injected to the each amplifier. Initial gate biases are shaped by the measured two-tone test depicted in the Fig. 1(b), and we have optimized the gate biases of the carrier and peaking amplifier in the



(a)



(b)



(c)

Fig. 2. (a) Simulated IMD characteristics with and without gate bias control. (b) Gate biases of the carrier and peaking amplifiers for optimizing the IMD3 characteristic. (c) Simulated ACLR performance of class-AB and Doherty amplifiers with and without gate bias control.

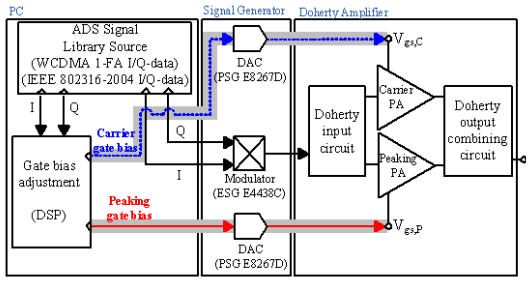


Fig. 3. Test bench for gate-bias envelope tracking.

experiment. Moreover, delay between gate bias and RF source path is adjusted by changing the length of cables and by altering the number of delay tap on the ADS simulator.

Fig. 4 shows the gate biases of the carrier and peaking amplifiers, which are shaped from the Fig. 1(b) and modified to maximize the linearity improvement, and WCDMA 1-FA envelope signal at the average output power of 33 dBm. From this figure, we can confirm delay between gate bias and RF source path don't exist. Fig. 5 shows the measured output spectra of the fixed and adapted gate bias for the Doherty PA at an average output power of 33 dBm. From the output spectra, we can recognize more linear characteristic of the proposed Doherty amplifier. Table 1 shows the summary of the measured performance for WCDMA 1-FA signal. Although the gate bias envelope tracking technique is in-

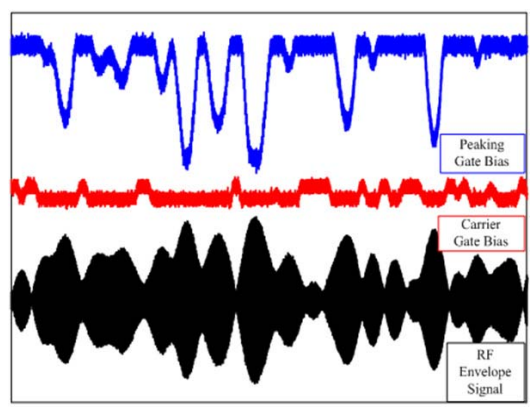


Fig. 4. Measured gate biases of the carrier and peaking amplifiers and envelope signal for WCDMA 1-FA signal.

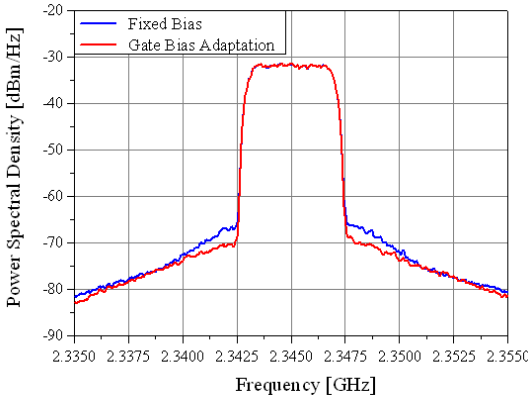


Fig. 5. Measured output spectra of the fixed and adapted gate bias for Doherty amplifier at average output power of 33 dBm.

Table 1. Summary of the measured performance at an average output power of 33 dBm for WCDMA 1-FA signal.

	Gain [dB]	PAE [%]	ACLR [dBc] +2.5/−2.5 MHz
Doherty (Fixed Bias)	14.3	25.6	−34.8/−35.0
Doherty (Bias Adaptation)	14.1	26.1	−37.4/−38.9

tended to enlarge the IM3 cancellation power range for linearity improvement, the PAE is also enhanced slightly due to the lower gate biases for the carrier and peaking amplifiers compared to the fixed gate bias Doherty amplifier.

Fig. 6 shows the gate biases of the carrier and peaking amplifiers and IEEE 802.16-2004 envelope signal at the average output power of 33 dBm. Figs. 7 show the measured signal constellation diagrams of the fixed and adapted gate bias for the Doherty amplifier at the average output power of 33 dBm. In comparison with the signal constellation diagram of the conventional Doherty amplifier, we can recognize the diagram of the gate bias controlled Doherty amplifier is clearer, which means the proposed Doherty amplifier can amplify the signal more linearly. Table 2 shows the summary of the measured performance for IEEE 802.16-2004 signal.

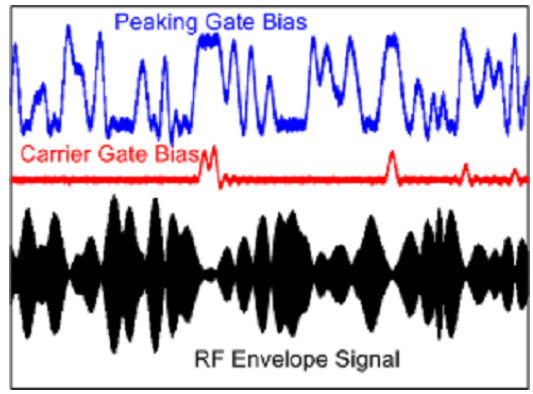


Fig. 6. Measured gate biases of the carrier and peaking amplifiers and envelope signal for IEEE 802.16-2004 signal.

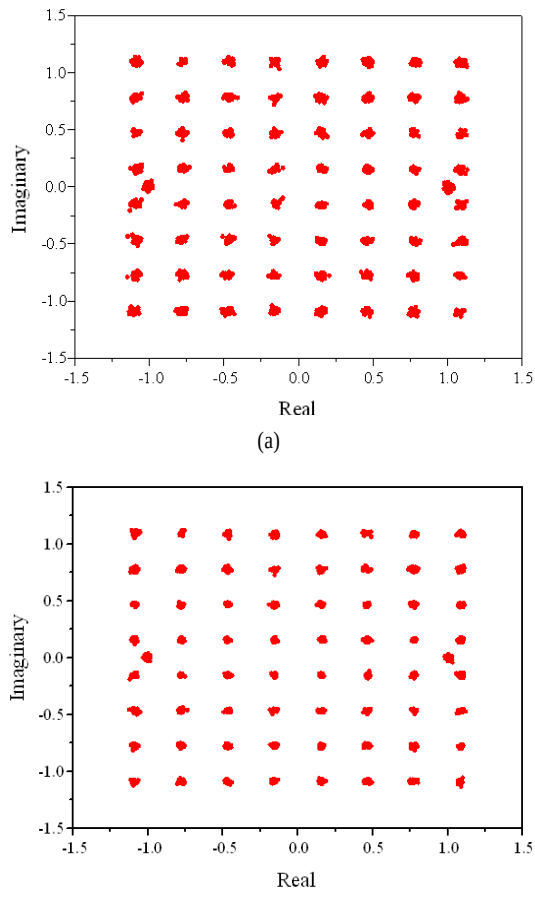


Fig. 7. Measured signal constellation diagram of (a) fixed gate bias and (b) controlled gate bias for the Doherty amplifier at the average output power of 33 dBm.

Table 2. Summary of the measured performance at an average output power of 33 dBm for IEEE 802.16-2004 signal.

	Gain [dB]	PAE [%]	RCE [dB]
Doherty (Fixed Bias)	14.3	25.6	−33
Doherty (Bias Adaptation)	14.1	25.4	−35

Ⅳ. Conclusion

We have implemented the gate-bias envelope tracking Doherty amplifier to improve the linearity performance. To extend the IM3 cancellation power regions, the proper gate biases are chosen through the two-tone test. Based on the measured gate biases according to the power levels, the dynamic gate bias adjustment of the carrier and peaking amplifiers is employed to maximize the harmonic cancellation. In the experiments, the gate-bias adapted Doherty amplifier delivers a lot more linear characteristic than the fixed gate-bias Doherty amplifier.

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