CMOS Linear Power Amplifier with Envelope Tracking Operation

(*Invited Paper*)

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Abstract

A differential-cascode CMOS power amplifier (PA) with a supply modulator for envelope tracking (ET) has been implemented by 0.18 μm RF CMOS technology. The loss at the output is minimized by implementing the output transformer on a FR-4 printed circuit board (PCB). The CMOS PA utilizes the 2nd harmonic short at the input to enhance the linearity. The measurement was done by the 10 MHz bandwidth 16QAM 6.88 dB peak-to-average power ratio long-term evolution (LTE) signal at 1.85 GHz. The ET operation of the CMOS PA with the supply modulator enhances the power-added efficiency (PAE) by 2.5, to 10% over the stand-alone CMOS PA for the LTE signal. The ET PA achieves a PAE of 36.5% and an $ACLR_{E-UTRA}$ of -32.7 dBc at an average output power of 27 dBm.

Key Words: CMOS, Envelope Tracking, Long-Term Evolution, Power Amplifier, Supply Modulator.

I. INTRODUCTION

The smartphone market has increased dramatically as smartphones have become an essential product in modern life. The increases in user demand for high quality service have prompted the evolution of wireless communication systems that can handle enormous amounts of data, which has required increased power consumption, efficient circuits, and large capacity batteries. The circuit cost and size are important parameters, so much research has been directed towards reducing the cost and size of smartphone elements. Among these elements, the front-end module is the bottleneck for these reductions. In this paper, we focus on radio frequency (RF) circuit systems and particularly on RF power amplifiers (PA).

Most of the chips in a smartphone are now being integrated into a single chip to reduce the size and cost. However, modifications to the RF power amplifier are lagging. Reliability and performance issues have led to the use of a gallium arsenide (GaAs) substrate for RF PA, whereas other chips are based on a CMOS substrate. The GaAs substrate has limited integration capability and high cost compared to the CMOS substrate; therefore, PAs will eventually be integrated into either a CMOS substrate with RFICs or a silicon-on-insulator (SOI) process with switches, for low cost and small size.

Silicon substrates have the drawbacks of a low breakdown voltage, no back via to the ground, a high knee voltage, and a large substrate loss. Even if the SOI process overcomes the substrate loss issue with a high-resistivity insulator beneath the buried oxide, the other issues must be taken care of at the circuit level, as in the bulk CMOS process [1, 2]. A

cascode structure provides a solution for a low breakdown voltage [3, 4]. A differential structure creates a virtual ground point and releases the source degeneration effect by a source-to-ground bonding wire [5]. The use of an output transformer helps to handle the substrate issues and the voltage combination also increases the output load impedance of transistors. The further improvement in the performance is achieved by the use of the appropriate harmonic tuning method described in this paper.

In addition to reducing the size and cost, improving the efficiency of the PA is also a hot issue. The PAs should handle the signals with wide channel bandwidth and high peak-to-average power ratio (PAPR) since the wireless communication systems, such as long-term evolution (LTE), operate using high data rate signals. The high PAPR of the signals reduces the efficiency of the PAs at a low average output power region because the fixed supply voltage and the output load are optimized for the peak instant power.

Several techniques can enhance the efficiency of PA for high PAPR applications. The Doherty technique modulates the load impedance using a quarter-wavelength transformer for both the back-off power and the peak power [6]. A reconfigurable output matching network, according to the power level, is also a good candidate for high PAPR signals [7]. However, these techniques require complex output matching networks, which have a large loss and are sensitive to a bandwidth. Envelope elimination and restoration (EER) and envelope tracking (ET) improve the efficiency by modulating the PA supply voltage. Conventional EER structures are nonlinear due to delay mismatch between the amplitude and the phase path, and further, they run into a leakage problem due to a large input power injection even for a low output operation [8]. The ET technique is less sensitive to the delay mismatch [9], and enables a linear operation by utilizing a linear PA and supply modulator without additional linearization technique [10] to improve the efficiency of the PA.

The organization of this paper is as follows. Section Ⅱ describes the harmonic control for the highly linear CMOS PA. Section Ⅲ shows the configuration of a hybrid switching supply modulator. Section Ⅳ focuses on the ET operation by combining the supply modulator and the CMOS PA. Implementation and measured results are shown in Section Ⅴ.

Ⅱ. Harmonic Control for Linear CMOS PA

Fig. 1 shows the schematic design of the CMOS PA with the hybrid supply modulator [10]. The basic structure of the PA is a differential-cascode structure that uses a transformer at the output [10−13]. This structure alleviates the drawbacks of the CMOS substrate. The performance is enhanced by designing the output transformer on a FR-4 printed circuit board (PCB) to minimize the loss. The 2nd harmonic short circuits are also applied at the input and output. Here, we have concentrated on the effects on the 2nd harmonic.
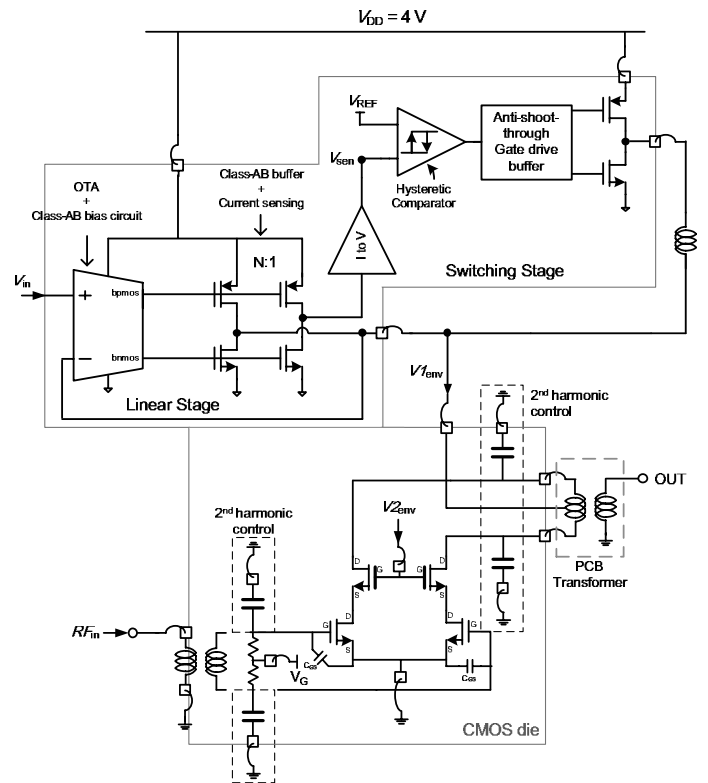

Fig. 1. Schematic of CMOS power amplifier with envelope tracking supply modulator. RF = radio frequency, PCB = printed circuit board, OTA = operational transconductance amplifier.

Many nonlinear components exist in a CMOS PA. As discussed in [14], C_{GS} contributes the most to linearity performance. Thus, compensating the C_{GS} nonlinearity is essential for improving the performance. The capacitance between the gate and source of the transistor increases as the voltage level increases across the two terminals, as shown in Fig. 2.

The RF PA gate bias is located in a class-AB mode. Fig. 2 shows the input voltage swing at the class-AB bias point,
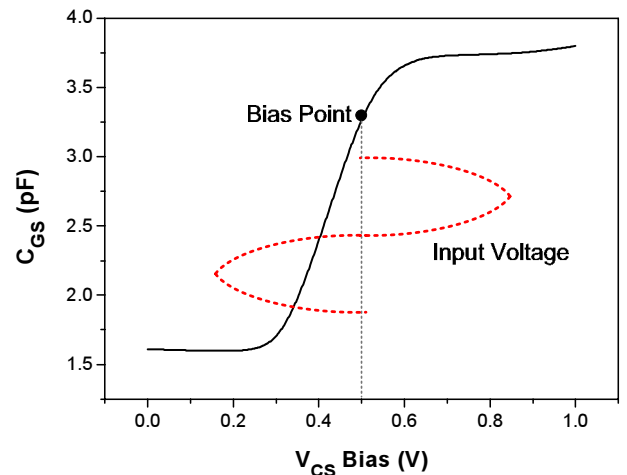

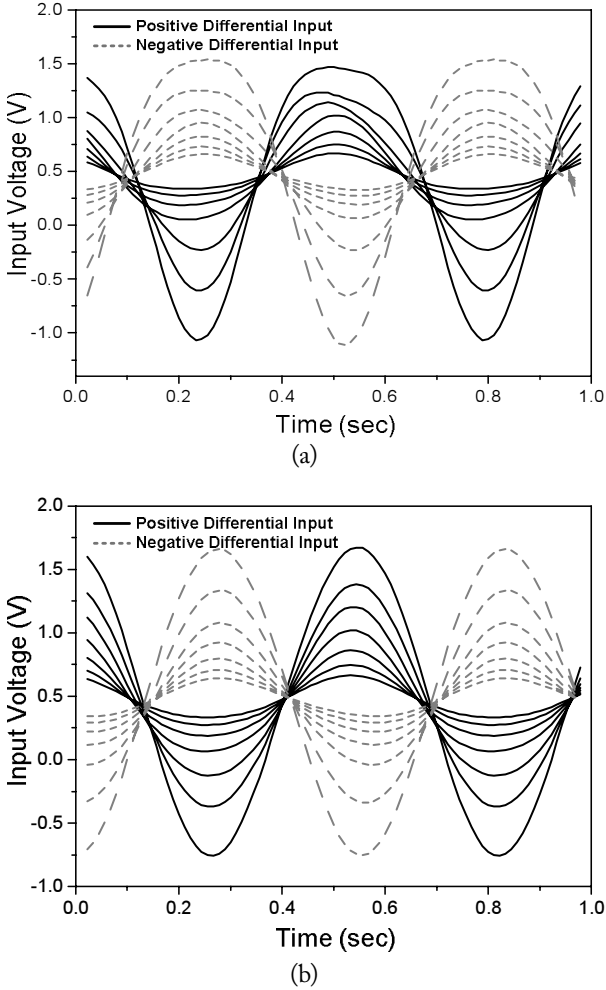Fig. 2. Variation of the gate to source capacitance.

Fig. 3. Simulated waveforms of input voltage according to input power levels: (a) without 2nd harmonic short and (b) with 2nd harmonic short.

Fig. 4. Simulated comparisons of third-order intermodulation distortion (IMD) between the power amplifiers with and without the 2nd harmonic short at the input.

together with C_{GS} variation. As clearly shown, the bias point is located where the C_{GS} varies rapidly. Therefore, the upper part of the input voltage and the lower part experience different capacitances and generate an asymmetric waveform, as plotted in Fig. 3(a). This asymmetric waveform is mainly due to the 2nd harmonic component that is generated by the nonlinear C_{GS}. Therefore, by applying the 2nd harmonic short circuit at the input, we can easily compensate the C_{GS} nonlinearity and achieve a symmetric waveform, as shown as Fig. 3(b). This symmetrical signal is especially important in a differential structure. This provides the proper virtual ground at the common source node of CS amplifiers, making a proper source ground. Additionally, this short eliminates the 2nd harmonic that is fed back to the input, which generates a memory effect. If not terminated, the 2nd harmonics can be mixed with the fundamental frequency signal, thereby creating the source of the asymmetry third-order intermodulation distortion (IMD3). Therefore, the 2nd harmonic short at the input is a very important linearizing element for a differential linear PA.
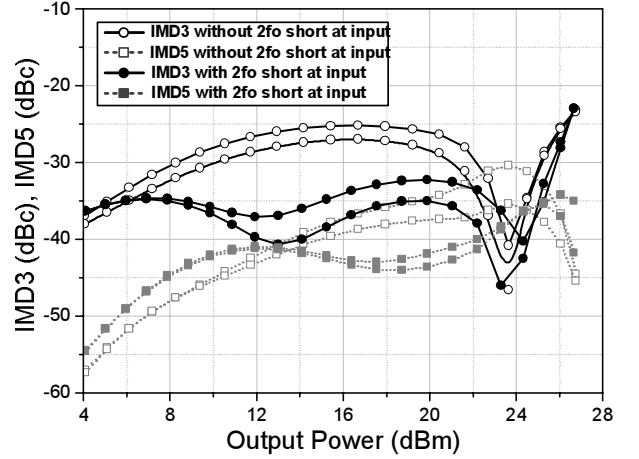
This effect was verified by carrying out a simulation. Two circuits are designed with and without input of the 2nd harmonic short. Both circuits are simulated with an output 2nd harmonic short and an ideal transformer. Fig. 4 shows the IMD curves with the 2nd harmonic short at the input, which clearly describes the effect of C_{GS} nonlinearity compensation. The IMD at the mid-power region is significantly reduced. Although the IMD at the high-power region is mainly generated by the nonlinearity caused by the voltage and current saturation [11], the linear output power, satisfying IMD3 below -30 dBc, has been increased by about 0.5 dB.

III. HYBRID SUPPLY MODULATOR DESIGN

A supply modulator is employed to modulate the drain bias of the RF PA for enhanced efficiency. Maximum efficiency of the ET system depends on the efficiency of both the PA and the supply modulator. In [15, 16], a low dropout regulator is employed as the supply modulator. It operates over a wide bandwidth, but is not efficient enough for high PAPR signals. In [17, 18], a switched-mode power supply (SMPS) delivers high efficiency, but its bandwidth is too narrow to use in 4G systems, such as Mobile-WiMAX and 3GPP LTE. In [19−21], a hybrid switching converter that combines the advantages of the two modulators is used to achieve high efficiency and good linearity simultaneously as shown in Fig. 5. In this architecture, the switching converter operates slowly as a quasi-constant current source, compared to a conventional SMPS, while the wideband linear regulator regulates the output voltage and compensates the ripple current of the switching converter. A control stage, which is composed of a current sensing circuit and a hysteretic comparator, changes the states of the switching converter according to the polarity and magnitude of the sensed current from the linear regulator to output.
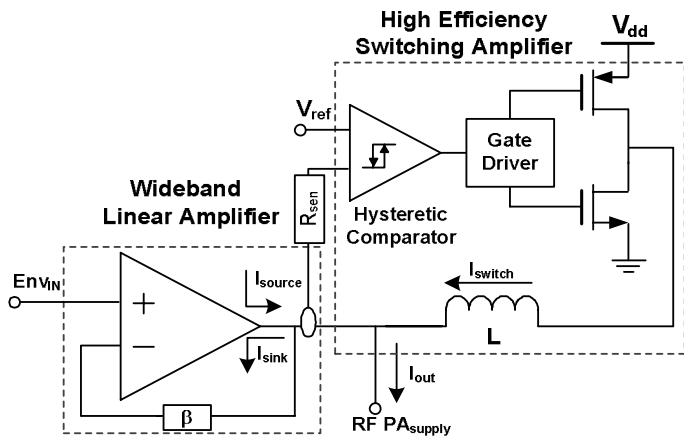
Fig. 5. Simplified block diagram of the hybrid supply modulator. RF = radio frequency, PA = power amplifier.

The wideband linear regulator operates as a voltage-controlled voltage source. This means the output voltage of the linear amplifier is the same as its input voltage due to its high gain, wide bandwidth, and negative feedback loop. As introduced in [21], a folded-cascode operational transconductance amplifier (OTA) is used as a gain stage to achieve a large bandwidth and a high DC gain. A large current driving capability and a rail-to-rail operation are obtained by an output buffer with a common source configuration, and it is biased at a class-AB for linearity and efficiency. The switching converter operates as a dependent current source. Generally, the average switching frequency is dependent on the hysteresis width, inductor value, and some other parameters for a narrowband signal.

The average switching frequency for a wideband signal is mainly determined by its bandwidth. The size of the power switch is determined by considering the conduction loss and switching loss at the specific load resistance. The protection, high efficiency, and low switching noise of the switches are obtained by using an anti-shoot-through circuit [22]. A gate driver for the anti-shoot-through switching converter turns on/off the two power transistors and can be designed easily using four MUXs and inverter chains [23].

The linear regulator determines the bandwidth of the supply modulator. The linear regulator of the designed supply modulator delivers a gain-bandwidth product of greater than 70 MHz and a DC gain of more than 50 dB with a stable operation. The dynamic output voltage swing range is from 0.9 to 3.5 V. The 0.9 V is the envelope shaping offset to prevent the operation below the knee voltage, and the 3.5 V is the peak envelope output voltage for a reliable operation of the CMOS RF PA. Fig. 6 shows a simulated efficiency of the supply modulators with a variable load. The variable load is a real PA model based on a class-AB biased PA and is realized by a voltage-controlled current source, as introduced in [21]. A 10-MHz LTE signal with a PAPR of 6.88 dB has a simulated efficiency of 78.5% at the peak power.
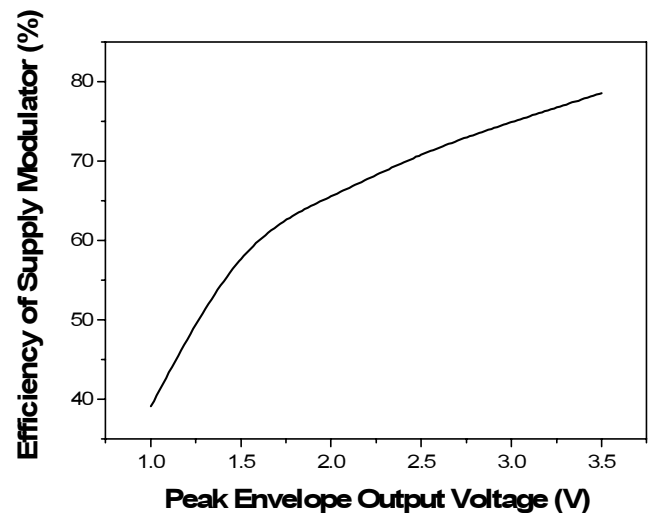

Fig. 6. Simulated efficiency of the supply modulator.

IV. CMOS PA with Envelope Tracking Operation

The PA under ET operation experiences large amplitude-to-amplitude modulation (AM/AM) and amplitude-to-phase modulation (AM/PM) distortions under a low supply voltage, since the input/output capacitance variations and the knee voltage effect are increased. Thus, the envelope signal is reshaped as shown in Fig. 7. The minimum voltage from the supply modulator is set to 0.65 V, and the envelope shape is decided according to the power level. Proper operation of the PA should be ensured by modulation of the gate of the common gate (CG) transistor as shown in the Fig. 7, to make the common source (CS) transistor and CG transistor stay in the saturation mode [4]. The envelope-shaping ensures that the PA operates at the IMD sweet spot tracked by the envelope of the signal, and the overall IMD is improved.

Fig. 8 shows the measured continuous wave performance of the PA at 1.85 GHz by sweeping the drain voltage from 1.0 to 3.5 V and the CG bias from 1.45 to 2.51 V. The
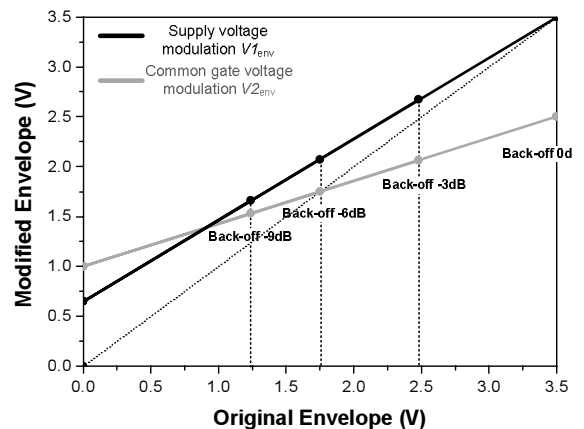

Fig. 7. Envelope-shaping for the voltages of the drain and the gate of the common-gate transistor.
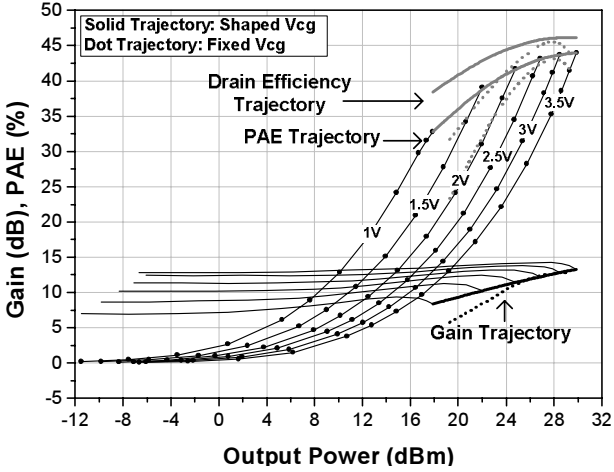
Fig. 8. Measured continuous wave performance of the power amplifiers sweeping the drain voltage from 1 to 3.5 V with the common gate (CG) bias V_{CG} swing from 1.45 to 2.51 V and fixed V_{CG}. PAE = power-added efficiency.

drain efficiency (DE), power-added efficiency (PAE), and gain of the PA for the LTE signal under ET operation are expected to follow the DE, PAE, and gain trajectories, respectively, as shown in the figure. For the sake of comparison, the performance for a fixed bias at the gate of the CG transistor is also plotted. The efficiency and the linearity are very poor for the fixed bias case. These data show that the properly shaped envelope shaping should also be supplied to the gate of the CG transistor for the ET operation with a cascode CMOS PA structure. The envelope shaping shown in Fig. 7 is optimized for the LTE signal at an output power of 27 dBm as well as at the back-off regions. In this way, the efficiency is improved significantly at a low power region.

V. IMPLEMENTATION AND EXPERIMENTAL RESULTS

The linear differential CMOS PA and ET supply modulator are fabricated on a 0.18-μm RF CMOS technology. Both chips are mounted on a FR-4 PCB. The output transformer is printed on the same board, having 0.5 dB loss. All inductors to resonate out the 2nd harmonics are realized by bonding wires to minimize the loss.

Fig. 9 shows the measured performance of the ET PA and the stand-alone PA at 1.85 GHz for a 10-MHz bandwidth 16QAM 6.88 dB PAPR LTE signal. The performance of the stand-alone PA with a supply voltage of 3.5 V results in a PAE of 34.0% and an ACLR$_{E-UTRA}$ of -30 dBc at an average output power of 27 dBm. The ET operation of the CMOS PA with the supply modulator enhances the PAE by 2.5% to 10% over the stand-alone CMOS PA for the LTE signal. The ET PA achieves a PAE of 36.5% and an ACLR$_{E-UTRA}$ of -32.7 dBc at an average output power of 27 dBm. Both the efficiency and linearity have been improved by ET operation. The measured average efficiency of the supply modulator under the LTE test is
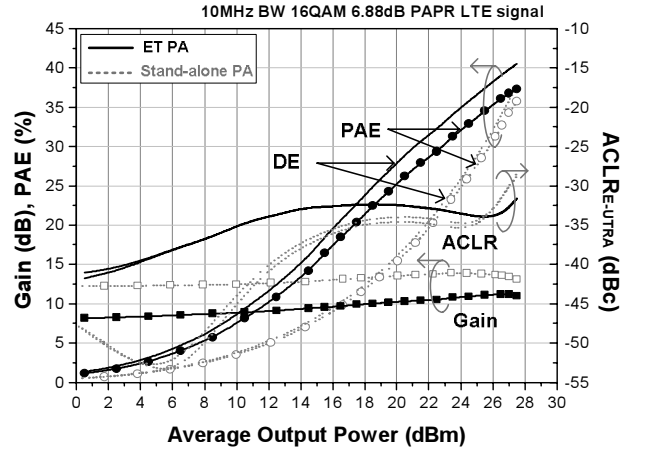

Fig. 9. Measured performance of the envelope tracking power amplifier (ETPA) and the stand-alone PA for a 10-MHz bandwidth 16QAM 6.88 dB peak-to-average power ratio long-term evolution signal. PAE = power-added efficiency, DE = drain efficiency, ACLR = adjacent channel leakage ratio.
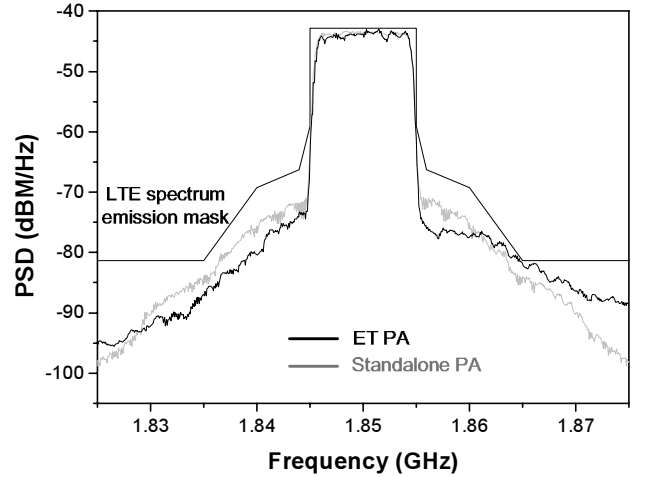

Fig. 10. Measured spectra of the power amplifier (PA) at an output power of 27 dBm for the long-term evolution (LTE) signal. ET = envelope tracking, PSD = power spectral density.
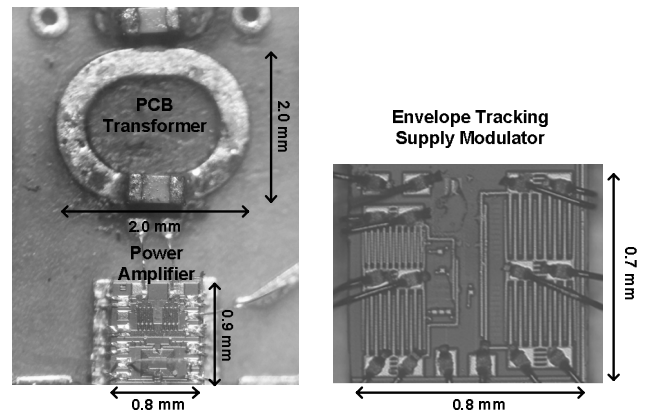

Fig. 11. The micrographs of the test chips and printed circuit board (PCB) transformer.

73%.

Fig. 10 depicts the measured spectra of the PAs at an output power of 27 dBm for the LTE signal. The ACLR$_{E-UTRA}$ is measured with a 9-MHz resolution bandwidth at both a center frequency and a 10-MHz offset and its specification is -30 dBc. Fig. 11 shows the micrographs of the supply modulator chip, the PA chip, and the PCB transformer. The total chip area sizes of the PA and supply modulator are 0.8 mm $\times$ 0.9 mm and 0.8 mm $\times$ 0.7 mm, respectively.

VI. Conclusions

A differential-cascode CMOS PA with supply modulator has been implemented by 0.18 μm RF CMOS technology. The importance in compensating the C$_{GS}$ has been described. The solution uses a 2nd harmonic short circuit. The efficiency of the PA system is improved by the introduction of a basic ET supply modulator. The supply modulator and the harmonic control on the PA help the ET PA to achieve a PAE of 36.5% and an ACLR$_{E-UTRA}$ of -32.7 dBc at an average output power of 27 dBm.

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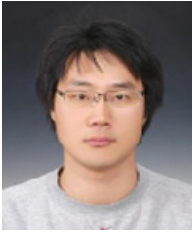
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